SIT Project

Action	ID	Faculty Name	Branch Name	Leave Type	From Date	To Date	Approved Days	Apply Days	Reason	HOD Approv
	40	Dilip krushnat patil	Electrical Engineering	sickkkkkkkkkkkk	18-07-2025	18-07-2025	1	1	ok	Approve
	39	Dilip krushnat patil	Electrical Engineering	sickness leave	18-07-2025	18-07-2025	1	1	ok	Approve
	38	Dilip krushnat patil	Electrical Engineering	sickkkkkkkkkkkk	18-07-2025	22-07-2025	0	5	ok	Process
	37	Dilip krushnat patil	Electrical Engineering	Sick Leave Record(SL)	18-07-2025	18-07-2025	0	1	ok	Process
	36	Dilip krushnat patil	Electrical Engineering	Casual Leave Record(CL)	24-07-2025	25-07-2025	0	2	Medical issues	Process
	35	Dilip krushnat patil	Electrical Engineering	Compensatory Holiday Record (CH)	20-07-2025	22-07-2025	0	3	Medical appoinemnt	Process
	34	Dilip krushnat patil	Electrical Engineering	Duty Leave Record(DL)	17-07-2025	17-07-2025	0	1	ssssss	Process
	33	Dilip krushnat patil	Electrical Engineering	Casual Leave Record(CL)	18-07-2025	19-07-2025	2	2	okkkk	Approve